



FORM PTO-1449	Atty. Docket No.: 03-1002/L13.12-0246	Appl. No.: 10/816,213	
LIST OF PATENTS AND PUBLICATIONS FOR APPLICANT'S INFORMATION DISCLOSURE STATEMENT		First Named Inventor:	
		Judy M. Gehman et al.	
		Filing Date	Group Art:
		April 1, 2004	

U.S. PATENT DOCUMENTS

Examiner Initial	Document No.	Date	Name	Class	Sub Class	Filing Date If Appropriate
	AA 6,574,778	06/2003	Chang et al.	716	1	
	AB 6,578,174	06/2003	Zizzo	716	1	
	AC 6,536,028	03/2003	Katsioulas et al.	716	17	
	AD 6,530,074	10/2002	Katsioulas et al.	716	17	
↓	AE 6,366,874	04/2002	Lee et al.	703	14	
	AF 6,334,207	12/2001	Joly et al.	716	17	

FOREIGN PATENT DOCUMENTS

		Document No.	Date	Country	Class	Sub Class	Translation Yes No
	AG						

OTHER ART (Including Author, Title, Date, Pertinent Pages, Etc.)

	AH	Sutherland, S.; "The IEEE Verilog 1364-2001 Standard What's New, and Why You Need It," 9th Annual International HDL Conference and Exhibition, March 2000. Pp. 1-8.
	AI	Cummings, C.; "Verilog-2001 Behavioral and Synthesis Enhancements," Revised April 2002, pp. 1-23.
	AJ	Cummings, C.; "New Verilog-2001 Techniques for Creating Parameterized Models (or Down with 'define' and Death of a defparam!) HDLCON 2002, pp. 1-10.
	AK	Wu, Y.; and MacDonald, P.; "Testing ASICs with Multiple Identical Cores," IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems, vol. 22, no. 3, March 2003, pp. 327-336.
↓	AJ	Miodrag Potkonjak et al. "Behavioral Synthesis of Area-Efficient Testable Designs Using Interaction Between Hardware Sharing and Partial Scan," IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems, vol. 14, no. 9, September 1995, pp. 1141-1154.
	AL	Chih-Chang Lin et al. "Test-Point Insertion: Scan Paths Through Functional Logic," IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems, vol. 17, no. 9, September 1998, pp. 838-851.

EXAMINER: /Satish Rampuria/ (04/13/2007)

DATE CONSIDERED:

EXAMINER: Initial if citation considered, whether or not citation is in conformance with MPEP 609; draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant.



FORM PTO-1449		Atty. Docket No.: 03-1002/L13.12-0246	Appl. No.: 10/816,213
LIST OF PATENTS AND PUBLICATIONS FOR APPLICANT'S INFORMATION DISCLOSURE STATEMENT		First Named Inventor:	
		Judy M. Gehman et al.	
		Filing Date April 1, 2004	Group Art:

U.S. PATENT DOCUMENTS

Examiner Initial	Document No.	Date	Name	Class	Sub Class	Filing Date If Appropriate
AM						
AN						
AO						
AP						
AQ						
AR						

FOREIGN PATENT DOCUMENTS

		Document No.	Date	Country	Class	Sub Class	Translation Yes No
	AS						

OTHER ART (Including Author, Title, Date, Pertinent Pages, Etc.)

	AT	Claus Schneider et al. "Modular Metrology Tools for Productivity Enhancement in Wafer Fabs," IEEE International Symposium on Semiconductor Manufacturing, Conference Proceedings, 1997. Oct. 6-8, 1997. Pp. B21-24.
	AU	Tianhao Zhang et al. "Design of Reconfigurable Composite Microsystems Based on Hardware/Software Codesign Principles," IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems, vol. 21, no. 8, Aug. 2002, pp. 987-995.
↓	AV	Ryota Kasai et al. "An Integrated Modular and Standard Cell VLSI Design Approach," IEEE Journal of Solid-State Circuits, vol. SC-20, no. 1, Feb. 1985 pp. 407-412.
	AW	Jeff Vanderlip. "LSI Logic Physical RTL Optimization (LSI PRO)," LSI Logic Corporation, Oct. 31, 2002. Pp. 1-7.

EXAMINER: /Satish Rampuria/ (04/13/2007) DATE CONSIDERED:

EXAMINER: Initial if citation considered, whether or not citation is in conformance with MPEP 609; draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant.